CLAIMS

WHAT IS CLAIMED IS:

1. A microprocessor comprising:

a translation lookaside buffer having a plurality of entries in which address translation information is registered, the address translation information being obtained by translating a virtual address into a physical address; and

a control circuit controlling said translation lookaside buffer, wherein:

each of the entries has a priority bit that is set when the registered address translation information is needed to be resident in the entries; and

at the time an entry substitution request occurs while priority bits of all of the entries are in a set state, said control circuit chooses as a subject of entry substitution an entry that has been least recently referred to, irrespective of states of the priority bits, the entry substitution being for substituting the registered address information in the entries.

2. The microprocessor according to claim 1, wherein

at the time the entry substitution request occurs while a priority bit in at least one of the entries is in a reset state, said control circuit chooses as a subject of entry substitution an entry that has been least recently referred to from the at least one of the entries.

3. The microprocessor according to claim 1, further comprising

a detection circuit detecting occurrence of continuous entry substitution requests under a single VLIW instruction, wherein

the microprocessor adopts a VLIW method in which a plurality of instructions contained in a single VLIW instruction are executed in parallel;

said translation lookaside buffer adopts a 2-way set associative method; and

said control circuit chooses as a subject of entry substitution an entry that has been previously referred to, irrespective of states of the priority bits, when said detection circuit

detects the occurrence of continuous entry substitution requests under a single VLIW instruction.

4. The microprocessor according to claim 3, wherein:

said detection circuit has: a holding circuit holding a storage address of a VLIW instruction corresponding to a most recent entry substitution; a comparator comparing the address held in said holding circuit and a storage address of a VLIW instruction corresponding to a present entry substitution; and a flag that is set when said comparator detects a match of the two addresses; and

while the flag is set, said control circuit chooses as a subject of entry substitution an entry that has been previously referred to, irrespective of states of the priority bits.

5. The microprocessor according to claim 4, wherein

said flag is reset in response to a transition of a storage address of a VLIW instruction.

6. The microprocessor according to claim 5, wherein:

said detection circuit includes an address detector detecting a transition of a storage address of a VLIW instruction; and

said flag is reset when said address detector detects a transition of a storage address of a VLIW instruction.

7. The microprocessor according to claim 4, further comprising

an interrupt controller managing a plurality of interrupt requests which are issued for interrupting execution of a program, wherein

said flag is reset in response to the interrupt controller's acceptance of an interrupt request not being an interrupt request for the entry substitution.

8. The microprocessor according to claim 7, wherein:

said interrupt controller includes an interrupt determining circuit determining a

factor of the accepted interrupt request; and

said flag is reset when said interrupt determining circuit determines that the accepted interrupt request is not a request for the entry substitution.